*Journal of Engineering Research and Reports*

***20(8): 38-44, 2021; Article no.JERR.69493***
***ISSN: 2582-2926***

# Defining an Optimized Machine Process Sequence to Address Broken Wafer Phenomenon on Semiconductor Products

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***Author's contribution***

*The sole author designed, analyzed, interpreted and prepared the manuscript.*

***Article Information***

DOI: 10.9734/JERR/2021/v20i817356
Editor(s):
(1) Dr. P. Elangovan, SRM TRP Engineering College, India.
Reviewers:
(1) Muryanto, Research Center for Chemistry – LIPI, Indonesia.
(2) Rudy Trisno M. T., Universitas Tarumanagara, Indonesia.
Complete Peer review History: http://www.sdiarticle4.com/review-history/69493

***Original Research Article***

***Received 06 April 2021***
***Accepted 10 June 2021***
***Published 12 June 2021***

## ABSTRACT

Silicon wafer as a direct material is one of the vital parts of a semiconductor product. Wastages on manufacturing plants that pulls the yield down should be addressed innovatively and accurately. This paper focused on the phenomenon of broken wafers at wafer taping process during wafer preparation. Using a wafer taper machine, silicon wafers are covered by an industrial tape as preparation for the next process. During processing and wafers are placed on wafer boat, unexpected phenomenon of broken wafers due to unwanted falling was encountered. Findings was due to the unintentional dragging of the machine's robot arm after wafer processing. The problem is resolved through simulation and experiments using statistical analysis. As a result, an optimized machine parameter setting was defined to eliminate the said rejection. Statistical analysis was of a big help in resolving the said phenomenon and improved the process yield of the manufacturing.

*Keywords: Integrated circuit; semiconductor; silicon wafer; wafer taping process.*

## 1. INTRODUCTION

Technology on our modern world cannot be denied having improved, adapted on our environment, and innovated continuously. Different products and services for humankind had been integrated by technological advancement in order to make our life easier,

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perform impossible jobs to be doable in a convenient way. Development continually derives our difficult tasks to an efficient and productive way of working, with consideration to high end and quality products and services. Different ways, procedures and disciplines were studied and strategically augmented to every individual on every way possible, as all around our progress relies on being productive with less waste, environmentally conscious, and quality focused on mind [1,2].

Semiconductor industries all over the world where integrated circuits are manufactured as we know are filled with experts and professionals in every sections of the manufacturing. They are focused and driven to improve all aspects of the manufacturing, from front of line stations where wafer sawing, die attach and wire bonding process takes place, up to end of line processes including encapsulation, unit singulation and laser marking [3-5]. These processes complete the integrated circuit with different applications depending on customers' demand.

Every process function with the help of industrial machines, which was built for the very purpose and requirement of every individual process. Parameters will be defined by machine experts during machine set up and come up with a processed product that will be used in the next process. Fig. 1 shows an example of a machine in semiconductor companies doing wafer taping/mounting, which cover silicon wafers by an industrial grade tape and undergo different processes to build integrated circuits. Depending on the machine's capability, its function is somehow limited on various material requirement and can be a cause of potential rejection of output units. this is the reason why determining appropriate parameters and process sequence is a prerequisite during development stage of the product [6-8].

The scope of discussion by this manuscript will be on the wafer taping process in the Front of line station inside semiconductor manufacturing. The process specified have been continuously developed by process experts in every manufacturing plants, as certain challenges were inevitably encountered during processing. Other works and studies related to wafer processing can be found in [9-13]. Tape and wafer related issues give negative fallouts that contributed to material rejections and loss of productivity because the process had to stop, and troubleshooting must be done. Broken silicon wafers, as shown on Fig. 2 caused by machine breakdown, malfunction, or unoptimized process defined, are one of them. These factors will result to scrappage of gross units and low process yield prior moving to the next process.

**Fig. 1. Wafer taper machine used in a semiconductor manufacturing**

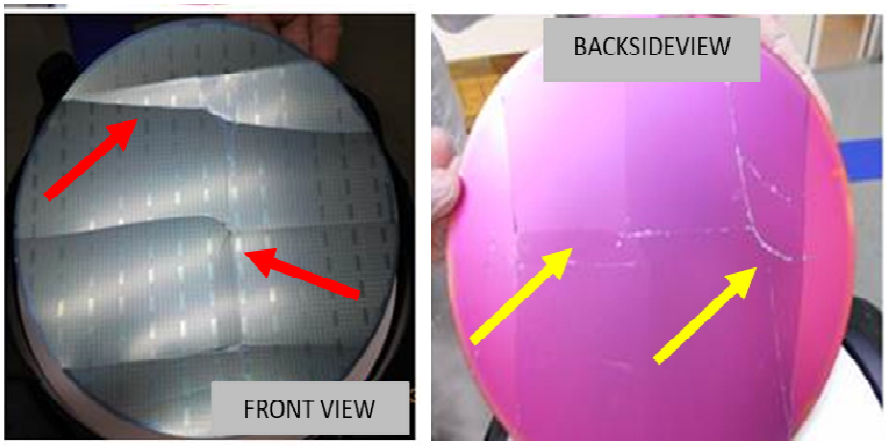


**Fig. 2. Broken silicon wafers in frontside and backside view**

Resolving this unwanted event had been the focus of this paper, having different options and sequence considered, and finalizing the appropriate actions to eliminate the occurrence of the said phenomenon.

## 2. METHODOLOGY

To determine the appropriate resolution of the said phenomenon, a detailed step by step process sequence is captured during the processing of wafers. Starting with loading of wafers on a wafer magazine or what we called "wafer boat" which hold a specific number of wafers to be processed located input section of the wafer taper machine. One wafer will be picked by the machine robot arm in a lateral position of the wafer and will be placed on the chuck table. A vacuum mechanism under the chuck table will activate upon start of the machine to hold the wafer in place. Two rollers carrying the wafer tape will pass through the wafer, covering the topside of the wafer to be processed. After covering, excess wafer tape beyond its diameter will be cut by a rotary blade cutter. After those sequences, the vacuum will disengage, and the covered wafer will then be picked again by the robot arm to place on the output wafer boat seated on the output area of the machine. This procedure will be repeated once all wafers from the input wafer boat has been processed by the taper machine.

As a default machine setting, Input wafer boat is being picked by the robot arm in bottom to top direction, and same also in placing processed wafers on the output wafer boat. As seen in Fig. 3, this machine setting is called "parallel", as the starting point of robot arm picking wafers from input and output wafer boat is from bottom to top direction. With this setting, unexpected phenomenon occurs such as broken wafers was encountered by the manufacturing. Theoretically, this parameter setting should be applicable to wafers aligned with its capability. The said issue was detected on the output area of the taper machine through series of snapshots and simulations as depicted in Fig. 4. It was found out that during robot arm retraction after placing the processed wafer, previous wafer below is dragged from the wafer boat and will fall unintentionally. This phenomenon eventually resulted to broken wafer rejection and must be resolved immediately to prevent recurrence and manufacturing yield losses.

## 3. RESULTS AND DISCUSSIONS

Experiments have been conducted to check possible solutions and derived with the best actions to address the said phenomenon. Wafer taper machine capability is considered also as it plays a big role in the experiment. Two available machine setting was compared and analyzed to define an optimized machine sequence that will also address the phenomenon. The other sequence considered aside from "parallel" is the "cross" setting. As shown in Fig. 5, the cross sequence starts on bottom to top direction on the input wafer boat, and top to bottom on the output wafer. Compared to parallel, this is literally a cross direction of the robot arm's sequence of picking and placing wafers from input to output. As seen also on Fig. 6, the cross setting eventually avoided the dragging of wafer because technically there is no wafer below.

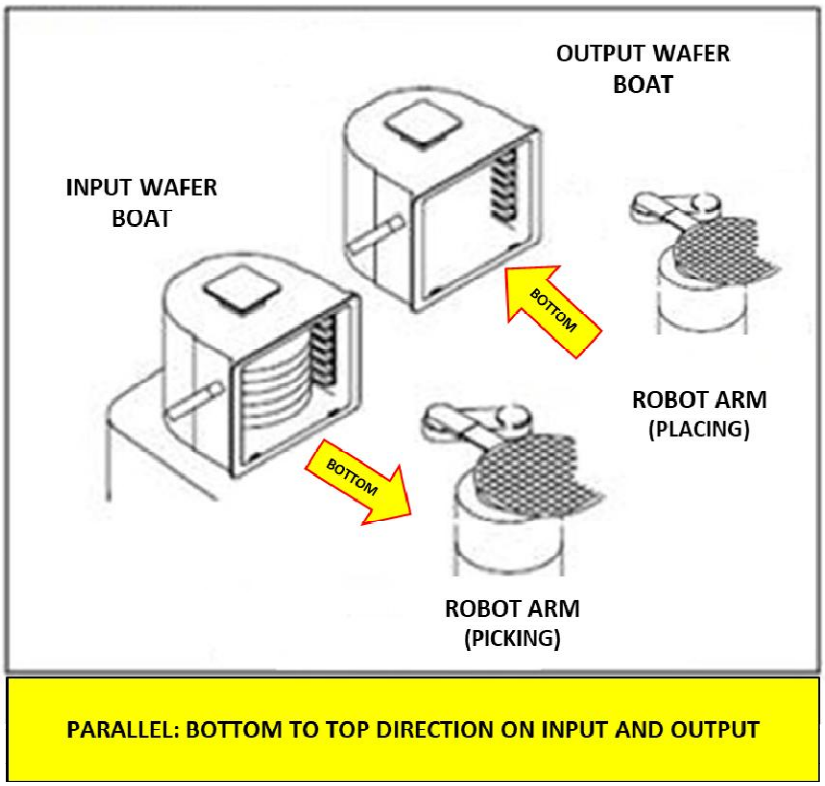


**Fig. 3. Parallel – Robot arm sequence in picking / placing of wafers**

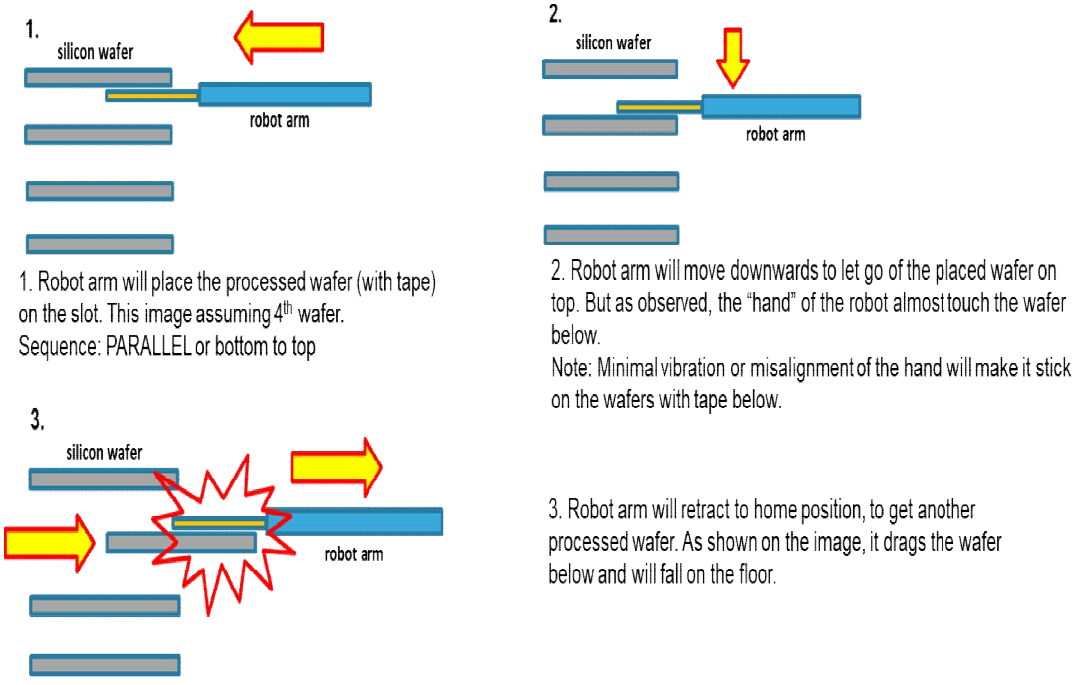


**Fig. 4. Parallel – Wafer robot sequence simulation on output module**

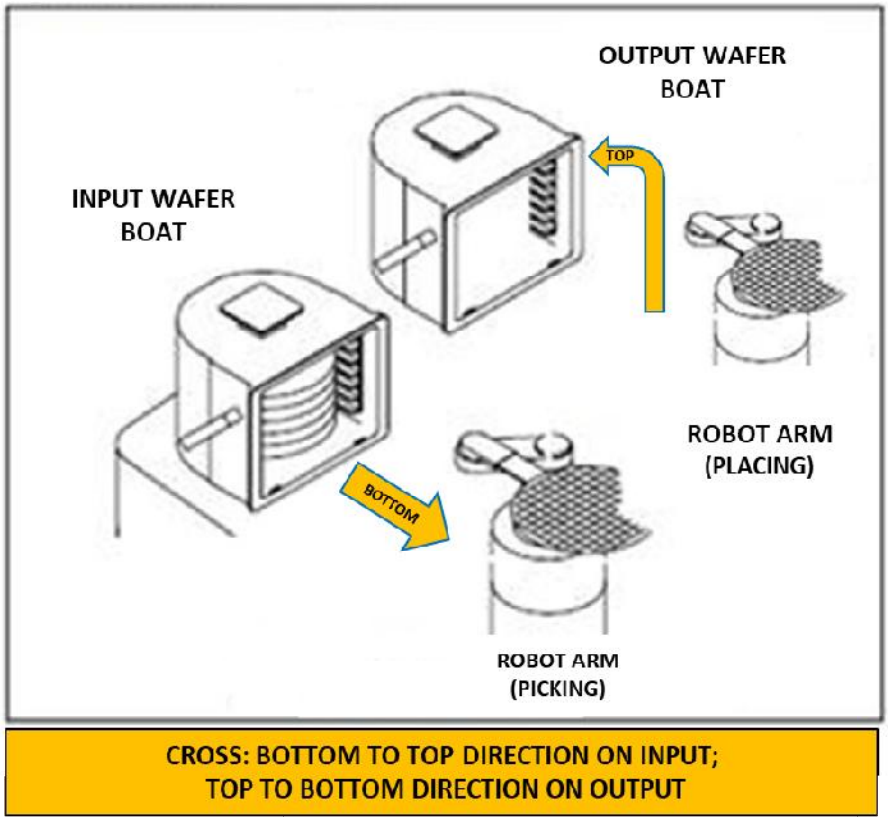


**Fig. 5. Cross – Robot arm sequence in picking / placing of wafers**

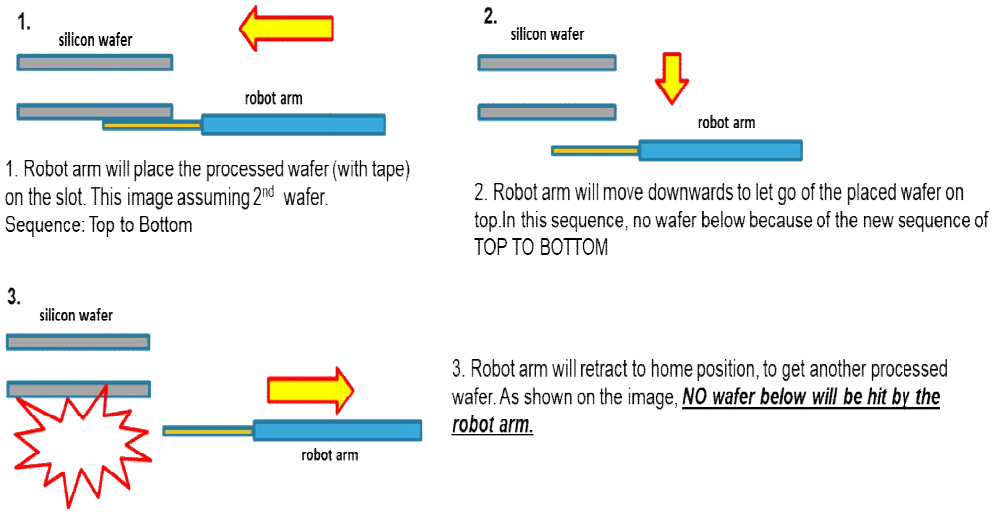


**Fig. 6. Cross – Wafer robot sequence simulation on output module**

Statistical tools shown in Fig. 7 were used to analyze the data from the experiment done. Gathering 50 data points: 25 from parallel and cross settings respectively, chi square on the 2-proportion test (A two proportion test allows you to compare two proportions to see if they are the same) indicates that these two settings are significantly different. Also, mosaic graph shows that cross setting shows positive result with no broken wafer recorded compared to parallel.


**Tests**

| N | DF | -LogLike | RSquare (U) |
|---|---|---|---|
| 50 | 1 | 4.5692514 | 0.2491 |

| Test | ChiSquare | Prob>ChiSq |
|---|---|---|
| Likelihood Ratio | 9.139 | 0.0025* |
| Pearson | 6.818 | 0.0090* |

| Fisher's Exact Test | Prob | Alternative Hypothesis |
|---|---|---|
| Left | 0.0111* | Prob(Run result=PASS) is greater for Machine setting=CROSS than PARALLEL |
| Right | 1.0000 | Prob(Run result=PASS) is greater for Machine setting=PARALLEL than CROSS |
| 2-Tail | 0.0223* | Prob(Run result=PASS) is different across Machine setting |

**Fig. 7. Statistical analysis of data from the experiment**

## 4. CONCLUSION AND RECOMMENDATIONS

Having this statistical analysis from the experiment conducted, defining the "cross" machine parameter setting is the optimized parameter, and eliminated the phenomenon of broken wafers on taping process. The study focused on the machine capability and contributed to an optimized machine setting with acceptable output response. The assesment done is significantly critical on manufacturing plants that targets zero material wastages and high product yield. Applying this kind of machine optimization evaluation is highly recommended on manufacturing plants with the same method of process or principle. Furthermore, innovations on related works and learnings stated on refereces cited would help to improve the process performance and robustness of wafer preparation process.

## DISCLAIMER

The company name used for this research is commonly and predominantly selected in our area of research and country. There is absolutely no conflict of interest between the authors and company because we do not intend to use this company as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the company rather it was funded by personal efforts of the authors.

## COMPETING INTERESTS

Author has declared that no competing interests exist.

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*Peer-review history:*
*The peer review history for this paper can be accessed here:*
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